PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Philip Mattos and Marco Losi
Application No.	:	10/632,566
Filed	:	August 1, 2003
For	:	INTEGRATED CIRCUIT FOR CODE ACQUISITION
	Examiner	: Ted M. Wang
	Art Unit	: 2611
	Docket No.	: 851963.411
	Date	: July 12, 2007

Mail Stop AF
Assistant Commissioner for Patents
Washington, DC 20231

SUPPLEMENTAL RULE 131 DECLARATION

Assistant Commissioner for Patents:

I, Ian M. Loveless, with a mailing address at Reddie & Grose, 16 Theobalds Road, London, WC1X 8PL, United Kingdom, declare as follows:

1. I am the UK patent attorney who filed European Patent Application No. 02255422.4 (hereinafter referred to as "the EP application") on August 2, 2002, upon which the application identified above (hereinafter referred to as "the present application") claims priority.

2. I previously executed a Rule 131 Declaration on April 2, 2007 (hereinafter referred to as "the first Loveless Rule 131 Declaration"), which based on my understanding, was filed with the U.S. Patent Office on April 10, 2007 during prosecution of the present application. This present Supplemental Rule 131 Declaration supplements the information provided in the first Loveless Rule 131 Declaration.

3. Paragraph 2 of the first Loveless Rule 131 Declaration discussed an "Exhibit 1," which was a transmittal letter from me to the inventor (Mr. Philip Mattos) transmitting a first draft of the EP application, prior to April 4, 2002. Exhibit 1A attached herewith is a copy of what I believe to be the first draft of the EP application, which describes one or more embodiments of the invention as disclosed to me by Mr. Mattos via meetings, notes,

and correspondence, prior to April 4, 2002. I believe this to be the first draft because the copy is dated prior to April 4 2002 in the handwriting of my secretary and so would have been the copy as retained in my file of the draft as sent to Mr. Mattos. The various manuscript amendments were written by me subsequent to the first draft.

4. Paragraph 3 of the first Loveless Rule 131 Declaration discussed my making subsequent revisions to the first draft of the EP application prior to April 4, 2002, including my working on the second draft of the EP application on March 28, 2002. This second draft of the EP application includes content and revisions based on invention disclosure information as provided to me by Mr. Mattos prior to April 4, 2002. Attached herewith as Exhibit 2A is what I believe to be a copy of the second draft of the EP application that embodies my said work of March 28, 2002, including the majority of the manuscript amendments on Exhibit 1A, which was then sent to Mr. Mattos for review on April 5, 2002 (along with a transmittal letter, a copy of which was previously presented as Exhibit 2 in the first Loveless Rule 131 Declaration).

5. I, together with my staff, filed the EP application on August 2, 2002. My understanding is that the present application claims priority based on that European application.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

16 August 2007
Date

Ian M. Loveless

701 Fifth Avenue, Suite 5300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

988730

EXHIBIT 1A

CODE ACQUISITION AND TRACKING

FIELD OF THE INVENTION

The present invention relates to the acquisition and tracking of broadcast pseudo random codes, in particular codes transmitted as part of a GPS signal.

BACKGROUND OF THE INVENTION

The Global Position System (GPS) is a well-known system which uses broadcast pseudo random codes to allow receivers to determine time differences, and hence relative positions, between a transmitter and receiver. The transmitters are satellites orbiting the earth in known orbit paths whose position at any given time is accurately known. Using received signals from four such satellites, a receiver can unambiguously determine its position using basic trigonometry to an accuracy dependent upon the repetition rate of the code, accuracy of components and other factors, such as the atmosphere and multipath reflections.

To increase accuracy, more than the minimum of four reference transmitters are usually tracked. There are around 24 satellites available for tracking in the GPS system, of which 8 are specified to be "visible" by a receiver at any given time. In fact, GPS receivers typically include 12 channels to allow up to 12 satellites to be tracked at once.

GPS satellites transmit two L-Band signals which can be used for positioning purposes. The reasoning behind transmitting using two different frequencies is so that

errors introduced by ionospheric refraction can be eliminated.

The signals, which are generated from a standard frequency of 10.23 MHz, are L1 at 1575.42 MHz and L2 at 1227.60 MHz and are often called the carriers.

The frequencies are generated from the fundamental satellite clock frequency of f_o = 10.23 MHz.

Signal	Frequency (MHz)	Wavelength (cm)
L1	$154f_o$ = 1575.42	~19
L2	$120f_o$ = 1227.60	~24

Since the carriers are pure sinusoids, they cannot be used easily for instantaneous positioning purposes and therefore two binary codes are modulated onto them: the C/A (coarse acquisition) code and P (precise) code.

Also it is necessary to know the coordinates of the satellites and this information is sent within the broadcast data message which is also modulated onto the carriers.

For purposes of imposing the binary data onto the carriers, all of the codes are transferred from the 0 and 1 states to the -1 and 1 factors respectively.

The coarse/acquisition (CA) code was so named as it was originally designed as a coarse position measurement signal on its own, or as an acquisition code to assist in looking onto the phase of the precise code. However, the CA code is now used generally both for acquisition and for position tracking, and so will be referred to simply as the CA code herein.

The C/A code is a pseudo random (PN) binary code (states of 0 and 1) consisting of 1,023 elements, or chips, that repeats itself every millisecond.

The term pseudo random is used since the code is apparently random although it has been generated by means of a known process, hence the repeatability.

Due to the chipping rate (the rate at which each chip is modulated onto the carrier) of 1.023Mbps, the chip length corresponds to approximately 300m in length and due to the code length, the ambiguity is approximately 300km - i.e. the complete C/A code pattern repeats itself every 300km between the receiver and the satellite.

The code is generated by means of a linear feedback register which is a hardware device representing a mathematical PN algorithm.

The sequences that are used are known as Gold codes which have particularly good autocorrelation and cross correlation properties. The cross correlation properties of the gold codes are such that the correlation function between two different sequences is low - this is how GPS receivers distinguish between signals transmitted from different satellites.

The receiver needs to know the actual position of satellites in addition to knowing its relative position to them, and for that reason a data message is broadcast. The data message includes information describing the positions of the satellites, their health status, ~~and the hand-over-word.~~

Each satellite sends a full description of its own orbit and clock data (within the ephemeris information) and an

approximate guide to the orbits of the other satellites (contained within the almanac information).

The data is modulated at a much slower rate of 50 bps and thus it takes 12.5 minutes to transmit all of the information. To reduce the time it takes to obtain an initial position, the ephemeris and clock data is repeated every 30 seconds. Parameters representing the delay caused by signal propagation through the ionosphere are also included within the data message.

The broadcast data message is modulo-2 added to ~~both~~ the C/A code ~~and the P code~~. This inverts the code and has the effect of also inverting the ~~auto~~correlation ~~function~~. signal after allowing the data to be received.

Binary biphase modulation (also known as binary phase shift keying [BPSK]) is the technique that is used to modulate the codes onto the initial carrier waves.

The codes are now directly multiplied with the carrier, which results in a 180 degree phase shift of the carrier every time the state of the code changes.

The modulation techniques also have the properties of widening the transmitted signal over a much wider frequency band than the minimum bandwidth required to transmit the information which is being sent ~~(Pratt, 1992)~~. This is known as spread spectrum modulation and has the benefits of developing processing gain in the despreading operation within the receiver, and it helps prevent possible signal jamming.

The L1 signal is modulated by both the C/A code and the P code, in such a way that the two codes do not interfere with each other. This is done by modulating one code in phase and the other in quadrature (i.e. they are at 90 degrees to each other).

$= \int_0^{2ms} carrier \times data \times CAcode \times CAcode + \int_0^{2ms} noise \times CAcode$

$= \int_0^{2ms} carrier \times data \times 1 + 0$

The C/A code is also amplified so that it is between 3 and 6 dB stronger than the P code.

A representation of the CA code, data message bits and the resultant signal spectrum is shown in Figure 1. As can be seen, the thermal noise level is higher than the actual signal level. In fact, the thermal noise is around -110dB per MHz, whereas the signal itself is around -130 dB. To extract the CA code from the noise, use is made of the fact that the CA code repeats itself every millisecond and correlation is performed. The function performed is to integrate the received signal with a locally generated version of the CA code, as follow:

$$\int_0^{2ms} [Signal + Noise) \times CA\ code$$

~~[Signal CA Code X Noise]~~

The result of the integration is that the noise component does not increase in signal level, but that CA code component is increased by 20,000 = +43dB. The CA code signal to noise ration is now +43dB (integration gain) - [-130 dB(signal) - 110dB(Noise)] = 23dB. The signal every ~~CA code~~ thereby becomes distinguishable from the noise.

A digital signal processor 10 for performing the above function is shown in Figure 2. Prior to digital processing, the received radio frequency (RF) signal is filtered with a radio chip (Figure 2a) to reject parts of the signal not in the L1 bandwidth (a filter with central frequency 1575 MHz and bandwidth ~~24~~ 2 MHz). The signal is then ~~modulated~~ mixed with a sinusoid generated by a local oscillator, resulting in the generation of a signal with ~~two~~ sum and different frequency components. A further filter of around 2 MHz bandwidth selects the

desired signal.

~~CA code~~. The signal produced is an IF signal which is sampled by the downconverter 12 at a rate defined by the clock generator 14 to convert to digital. The rate is typically a multiple of 1.023 MHz which is the CA code chip rate (in this case 4.092 MHz).

The signal is then copied and sent into 12 separate channels 16, each channel being arranged to extract the code and carrier information for a particular satellite. A replica of the CA code for the particular satellite is generated by a prn 18 and correlated with the signal in each channel 16. ~~Three~~ two replica codes are actually used for the correlations; ~~one directly aligned with the IF signal (punctual)~~, one delayed (late) and one advanced (early). The early and late codes lie on the slope of the ~~auto~~correlation function either side of the peak, and are used in continuous tracking of the code to reduce tracking error. The signal is then processed for the data modulation and carrier phase measurements. A locally generated carrier is generated by a numerically controlled oscillator (NCO) 22 and a second downconverter 20 used to reject images prior to an output block 24.

When correlating to acquire the signal the time and hence phase of the incoming signal is an unknown. It is necessary, therefore, to compare 2 x 1,023 = 2,046 acquisition samples of the CA code signal for every possible relative position of the incoming and locally generated CA codes, with an integration period of 1 millisecond typically. It thus takes around 2 seconds to acquire the first satellite. Thereafter the position of the sequence is known and tracking requires ~~far fewer~~ only two comparisons, correlations, rather than 2046, tracking to ~~verify that~~ maintain the position ~~remains~~ within a ~~1 μs to +1 μs~~ window of the early and late measurements. nanoseconds.

~~For using code~~ using one channel.

We have appreciated the need for a large number of correlations for acquisition of signals, but only a few correlations to track the signals after acquisition. We

have further appreciated disadvantages of known solutions which use large numbers of correlators.

SUMMARY OF THE INVENTION

The invention is defined in the claims to which reference is now directed.

A circuit embodying a first aspect of the invention samples a received signal by combining received digitised signal bits in a ~~code~~ prior to correlation, thereby speeding the correlation process.

A ~~second~~ circuit embodying a second aspect of the invention increases the speed of correlation by correlating a received signal at a multiple of the usual speed by reading received data from one buffer store whilst writing new received data to another buffer store.

BRIEF DESCRIPTION OF THE FIGURES

An embodiment of the invention will now be described by way of example only and with reference to the accompanying figures, in which:

Figure 1: is a representation of a repeated CA code as used in the present invention and its signal spectrum;

Figure 2: shows a known signal processor ~~which may embody the invention~~;

Figure 2a shows a radio chip

Figure 3: shows a semiconductor circuit embodying the invention;

Figure 4: shows an alternative semiconductor circuit embodying the invention;

Figure 5: shows a code generator for use in the circuits of Figures 3 or 4;

Figure 6: shows an edge correlator truth table; and

Figure 7: shows edge correlator waveforms.

Figure 4 shows an arrangement of a decimator;
Figure 5 shows the sampling of the signal;
Figure 6 shows an alternative decimator;

Add change to 12 channels to 16 channels.

* The first down converter 12 is shown in expanded view in figure 2a. The received signal is filtered and then digitised by sampling at 16MHz (in fact 16.368MHz) to produce - 8 - a digital output.

DESCRIPTION OF A PREFERRED EMBODIMENT

The embodiment of the invention is a digital signal processor (DSP) 10 for GPS signal acquisition and tracking as previously described in relation to Figure 2, but modified to include additional functionality, which is operable to increase the speed of signal acquisition. The DSP 10 shown in Figure 2 comprises a signal input to a first down converter 12, as previously described, which converts a received IF signal containing a repeated code input to digital at the sampled rate defined by clock generator 14 (1.023 MHz). The digital signal is then provided to a series of ~~12~~ 16 channels 16, each used to track one of up to ~~12~~ 16 satellites simultaneously in a tracking mode. In tracking mode the respective CA code for a given satellite is fed to the respective channel 16 from a code generator shown as prn 18. In acquisition mode, all ~~12~~ 16 channels ~~are~~ may be initially used to acquire the first satellite signal, thereafter each channel tracks the respective satellite.

(*) An alternative embodiment using only a single shift register is shown in figure X.

(A) ~~The pertinent parts of the digital signal processor embodying the invention are shown in Figure 3, which shows the channels 16 in greater detail~~. Although not shown, there are ~~12~~ 16 separate correlators - one for each channel. Also, the figure only shows one of the inphase (I) and quadrative (Q) channels for simplicity.

(B) ~~An incoming signal containing a CA code is clocked into the channel 16 at a frequency derived from a gate 42 and NCO 40 by gate 44. The clocking in frequency is derived from an input 4.092 MHz clock, and is preferably 2.046 MHz (twice the CA code chip rate).~~ A decimator 26 comprises combinatorial logic to combine groups of 8 samples to reduce the sample rate without discarding information. It is noted, for the avoidance of doubt, that the decimation is not simply removing every 10th sample. The decimated

~~at for example 4MHz is~~ ~~decimation in gate 44~~ The received signal ~~An incoming signal~~ ~~shift register~~ ~~derived from a 16MHz~~ as before

An incoming signal is mixed ~~down~~ by gate 44, ~~and~~ fed with a locally generated 4.092MHz.

signal is loaded to a shift register 28 having multiple taps 29 which feed to correlators 30. The shift register is operable, when loaded, to circulate at a higher speed than the loading speed, such as 66 MHz or 200 MHz. Each tap 29 feeds a separate correlator 30 (only one being shown for simplicity). A code generator 36 generates a local version of the respective CA code and applies this to the correlator 30. The correlator includes combinatorial logic 32 which combines the local version of the CA code with the decimated received signal from the tap points 29 of the circulating shift register. A low pass filter 34 provides the output.

The operation of the channel 16 is in two modes; an acquire mode and a tracking mode. The acquire mode will be described first. On first receiving a satellite signal which has been sampled at ~~1.023 MHz~~, the timing of the satellite which sent the signal and the relative distance are both unknowns. Accordingly, it is necessary to perform 2,046 (2x1,023 chips of the CA code) comparisons to determine the relative time difference between the local version of the CA code and the received signal. The received signal is first decimated, though, to reduce the samples by a factor of 8. The decimated samples are fed to the shift register at 2.046 MHz which then circulates at a higher speed such as 66 MHz or 200 MHz. Each of ~~12~~ tap points 29 is fed to a respective correlator 30. The ~~12~~ correlators 30 each receive the same CA code for a given satellite from the code generator ~~30~~. There are thus effectively ~~12~~ correlators running in parallel on a signal which is reduced by a factor of 8 samples at a speed which is a multiple of the usual speed. If the speed is 66 MHz, this is 4 times faster than usual so the system is 4 x 8 = 32 times faster than ~~12~~ channels without decimation or the high speed register. If the speed is 200 MHz, this is 12 times faster than usual so that system

(*) whilst the second embodiment cannot operate to perform all possible correlations in real time (because the received digitised data will be at a faster rate than the correlations) the single shift register embodiment still provides a some speed advantage.

is 12 x 8 = 96 times faster than ~~12~~ 16 channels without decimation on the high speed register.

The increase in speed means either a faster acquisition or more sensitivity in the same time. For example, 32 times faster means 32 times more sensitive at the same acquisition speed giving around 15 dB gain.

When the signal has been acquired (the relative time difference has been calculated by the correlations) there is less need for high speed correlation. Accordingly, the channels enter a second mode; the tracking mode. In this mode the decimator 26 no longer decimates the incoming signal ~~to preserve accuracy to within 1 chip of the CA code~~ by correlating the. The code generator 36 now supplies a different respective code to each of the ~~12~~ 16 correlators; one for each respective satellite to be tracked. The relative positions of the incoming and local signal are now known to a degree of accuracy of ~~several chips~~ a few nanoseconds rather than being unknown and so can be tracked using the early and late signals discussed before ~~and described more fully later~~.

(*) move to (A)

An embodiment of the invention is shown in Figure ~~4~~ 3 and comprises ~~input combinatorial logic~~ a Mixer 44 ~~clocked at~~ fed with locally generated 4.092MHz which connects to a decimator 26 ~~as before~~. A pair of shift registers 50, 51 receive the output from the decimator and connect to a multiplexer 52 which feeds to 16 channels 30 each comprising a local code generator, shown as PRN 36 multiplexed 32 and a low pass filter 34.

STET

keep this!

The operation of the embodiment is as follows. The down converted, digitised received, and ~~A to D converted~~ GPS signal is ~~first~~ decimated by the decimator 26. Preferably, this is by producing a combinatorial output from groups of 8 samples, thereby reducing the sample rate by a factor of 8. Then the decimated samples are loaded into a first shift register 50 at a rate of 2.046 MHz. When the first shift

expand all instances

M x N

The factor M is the number of samples shifted into the decimator.

register 50 is full, the input is switched to the second shift register 51 and the output of the first shift register 50 is directed by multiplexer 52 to the channels 30. The output of the first shift register is also looped back to its input. The first shift register is then circulated at a higher than normal frequency, such as 128 MHz. In each channel 30 a PRN generator 36 generates a local version of the CA code and a ~~combinational element~~ multiplier 32 combines the decimated received code with the local version of the CA code. The clock of the correlators and first shift register run at the same multiple of the normal rate thereby performing many searches on the data before the second shift register 51 is full. At which point, the input is switched to the first register 50 and the multiplexer 52 switches the output of the second register 51 to the correlators.

Note the special case when the sample rate reduction, the overclocking, and the number of correlators combine to allow processing at 2046 or more times real time rate. Then all possible time-domain searches can be performed before switching buffers, so no data is lost and the correlator outputs can be further integrated by hardware or software accumulators, completely separating the integration period (and hence sensitivity) from the size of the input buffers. This greatly enhances sensitivity and reduces silicon area.
Example implementation x8 decimation, x8 clock, x16 channels, x2 correlators per channel is x 2048 real time.

The hardware can thereby perform all 2046 correlations in 1ms which is the repeat period of the CA code. This means that every 1 ms when the code repeats it can be correlated for all possible time domains.

The shift registers described could equally be implemented by other stores such as RAM with counters for addressing.

Any buffer store which is capable of reading in at a first rate and reading out a sequence of digital data at a second higher rate will do.

Figures 5, 6 and 7 show the use of combinatorial components for tracking using early and late signals as previously mentioned. [Is this part of the invention, or well-known? If well-known, there is probably no reason to describe this].

EXHIBIT 2A

01-IMS-018x019

CODE ACQUISITION AND TRACKING

FIELD OF THE INVENTION

The present invention relates to the acquisition and tracking of broadcast pseudo random codes, in particular codes transmitted as part of a GPS signal.

BACKGROUND OF THE INVENTION

The Global Position System (GPS) is a well-known system which uses broadcast pseudo random codes to allow receivers to determine time differences, and hence relative positions, between a transmitter and receiver. The transmitters are satellites orbiting the earth in known orbit paths whose position at any given time is accurately known. Using received signals from four such satellites, a receiver can unambiguously determine its position using trigonometry to an accuracy dependent upon the repetition rate of the code, accuracy of components and other factors, such as the atmosphere and multipath reflections.

To increase accuracy, more than the minimum of four reference transmitters are usually tracked. There are around 24 satellites available for tracking in the GPS system, of which 8 are specified to be "visible" by a receiver at any given time. In fact, GPS receivers typically include 12 channels to allow up to 12 satellites to be tracked at once.

GPS satellites transmit two L-Band signals which can be used for positioning purposes. The reasoning behind transmitting using two different frequencies is so that

errors introduced by ionospheric refraction can be eliminated.

The signals, which are generated from a standard frequency of 10.23 MHz, are L1 at 1575.42 MHz and L2 at 1227.60 MHz and are often called the carriers.

The frequencies are generated from the fundamental satellite clock frequency of f_o = 10.23 MHz.

Signal	Frequency (MHz)	Wavelength (cm)
L1	$154f_o$ = 1575.42	~19
L2	$120f_o$ = 1227.60	~24

Since the carriers are pure sinusoids, they cannot be used easily for instantaneous positioning purposes and therefore two binary codes are modulated onto them: the C/A (coarse acquisition) code and P (precise) code.

Also it is necessary to know the coordinates of the satellites and this information is sent within the broadcast data message which is also modulated onto the carriers.

For purposes of imposing the binary data onto the carriers, all of the codes are transferred from the 0 and 1 states to the -1 and 1 factors respectively.

The coarse/acquisition (CA) code was so named as it was originally designed as a coarse position measurement signal on its own, or as an acquisition code to assist in looking onto the phase of the precise code. However, the CA code is now used generally both for acquisition and for position tracking, and so will be referred to simply as the CA code herein.

The C/A code is a pseudo random (PN) binary code (states of 0 and 1) consisting of 1,023 elements, or chips, that repeats itself every millisecond.

The term pseudo random is used since the code is apparently random although it has been generated by means of a known process, hence the repeatability.

Due to the chipping rate (the rate at which each chip is modulated onto the carrier) of 1.023Mbps, the chip length corresponds to approximately 300m in length and due to the code length, the ambiguity is approximately 300km - i.e. the complete C/A code pattern repeats itself every 300km between the receiver and the satellite.

The code is generated by means of a linear feedback register which is a hardware device representing a mathematical PRN algorithm.

The sequences that are used are known as Gold codes which have particularly good autocorrelation and cross correlation properties. The cross correlation properties of the gold codes are such that the correlation function between two different sequences is low - this is how GPS receivers distinguish between signals transmitted from different satellites.

The receiver needs to know the actual position of satellites in addition to knowing its relative position to them, and for that reason a data message is broadcast. The data message includes information describing the positions of the satellites and their health status.

Each satellite sends a full description of its own orbit and clock data (within the ephemeris information) and an approximate guide to the orbits of the other satellites (contained within the almanac information).

The data is modulated at a much slower rate of 50 bps and thus it takes 12.5 minutes to transmit all of the information. To reduce the time it takes to obtain an initial position, the ephemeris and clock data is repeated every 30 seconds. Parameters representing the delay caused by signal propagation through the ionosphere are also included within the data message.

The broadcast data message is modulo-2 added to the C/A code. This inverts the code and has the effect of also inverting the signal after correlation allowing the data to be recovered.

Binary biphase modulation (also known as binary phase shift keying [BPSK]) is the technique that is used to modulate the codes onto the initial carrier waves.

The codes are now directly multiplied with the carrier, which results in a 180 degree phase shift of the carrier every time the state of the code changes.

The modulation techniques also have the properties of widening the transmitted signal over a much wider frequency band than the minimum bandwidth required to transmit the information which is being sent. This is known as spread spectrum modulation and has the benefits of developing processing gain in the despreading operation within the receiver, and it helps prevent possible signal jamming.

The L1 signal is modulated by both the C/A code and the P code, in such a way that the two codes do not interfere with each other. This is done by modulating one code in phase and the other in quadrature (i.e. they are at 90 degrees to each other).

A representation of the CA code, data message bits and the resultant signal spectrum is shown in Figure 1. As can be seen, the thermal noise level is higher than the actual signal level. In fact, the thermal noise is around -110dB per MHz whereas the signal itself is around -130 dB. To extract the CA code from the noise, use is made of the fact that the CA code repeats itself every millisecond and correlation is performed. The function performed is to integrate the received signal with a locally generated version of the CA code, as follow:

$$\int_0^{2ms} (\text{signal} + \text{noise}) \times \text{CA code}$$

$$= \int_0^{2ms} \text{carrier} \times \text{data} \times \text{CA code} \times \text{CA code}$$

$$+ \int_0^{2ms} \text{noise} \times \text{CA code} = \int_0^{2ms} \text{carrier} \times \text{data} \times 1 + 0$$

The result of the integration is that the noise component does not increase in signal level, but that CA code component is increased by 20,000 = +43dB. The CA code signal to noise ratio is now:

+43dB (integration gain) - [-130 dB(signal) - 110dB(Noise)] = 23dB. The signal energy thereby becomes distinguishable from the noise.

A digital signal processor 10 for performing the above function is shown in Figure 2. Prior to digital processing, the received radio frequency (RF) signal is filtered within a radio chip (Figure 2a) to reject parts

of the signal not in the L1 bandwidth (a filter with central frequency 1575 MHz and bandwidth 20 MHz). The signal is then mixed with a sinusoid generated by a local oscillator, resulting in the generation of a signal with sum and difference frequency components. A further filter of around 2 MHz bandwidth selects the desired signal. The signal produced is an IF signal which is sampled by the downconverter 12 at a rate defined by the clock generator 14 to convert to digital. The rate is typically a multiple of 1.023 MHz which is the CA code chip rate (in this case 4.092 MHz).

The signal is then copied and sent into 12 separate channels 16, each channel being arranged to extract the code and carrier information for a particular satellite. A replica of the CA code for the particular satellite is generated by a prn 18 and correlated with the signal in each channel 16. Two replica codes are actually used for the correlations; one delayed (late) and one advanced (early). The early and late codes lie on the slope of the correlation function either side of the peak, and are used in continuous tracking of the code to reduce tracking error. The signal is then processed for the data modulation and carrier phase measurements. A locally generated carrier is generated by a numerically controlled oscillator (NCO) 22 and a second downconverter 20 used to reject images prior to an output block 24.

When correlating to acquire the signal the time and hence phase of the incoming signal is an unknown. It is necessary, therefore, to compare 2 x 1,023 = 2,046 acquisition samples of the CA code signal for every possible relative position of the incoming and locally generated CA codes, with an integration period of typically 1 millisecond. It thus takes around 2 seconds to acquire the first satellite using one channel. Thereafter the position of the sequence is known and

tracking requires only two correlations, rather than 2046, to maintain the tracking position within a nanosecond window of the early and late measurements.

We have appreciated the need for a large number of correlations for acquisition of signals, but only a few correlations to track the signals after acquisition. We have further appreciated disadvantages of known solutions which use large numbers of correlators.

SUMMARY OF THE INVENTION

The invention is defined in the claims to which reference is now directed.

A circuit embodying a first aspect of the invention samples a received signal by combining bits in a received digitised signal prior to correlation, thereby speeding the correlation process.

A circuit embodying a second aspect of the invention increases the speed of correlation by correlating a received signal at a multiple of the usual speed by reading received data from one buffer store whilst writing new received data to another buffer store.

BRIEF DESCRIPTION OF THE FIGURES

An embodiment of the invention will now be described by way of example only and with reference to the accompanying figures, in which:

Figure 1: is a representation of a repeated CA code as used in the present invention and its signal spectrum;
Figure 2: shows a known signal processor;
Figure 2a: shows a radio chip;

Figure 3: shows a semiconductor circuit embodying the invention;

Figure 4: shows one arrangement of a decimator;

Figure 5: shows the sampling of the signal;

Figure 6: shows an alternative decimator; and

Figure 7: shows an alternative semiconductor circuit embodying the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

The embodiment of the invention is a digital signal processor (DSP) 10 for GPS signal acquisition and tracking as previously described in relation to Figure 2, but modified to include additional functionality, which is operable to increase the speed of signal acquisition. The DSP 10 shown in Figure 2 comprises a signal input to a first down converter 12, as previously described, which converts a received IF signal containing a repeated code input to digital at the sampled rate defined by clock generator 14 a multiple of (1.023 MHz). The digital signal is then provided to a series of 16 channels 16, each used to track one of up to 16 satellites simultaneously in a tracking mode. In tracking mode the respective CA code for a given satellite is fed to the respective channel 16 from a code generator shown as prn 18. When adapted to embody the invention, in acquisition mode, all 16 channels may be initially used to acquire the first satellite signal, thereafter each channel tracks the respective satellite.

The first down converter 10 is shown in expanded view in Figure 2a. The received signal is filtered and then digitised by sampling at 16 MHz (in fact 16.368MHz) to produce a digital output.

An embodiment of the invention is shown in Figure 3 and comprises a mixer 44 fed with locally generated 4.092 MHz

which connects to a decimator 26. A pair of shift registers 50, 51 receive the output from the decimator and connect to a multiplexer 52 which feeds to 16 channels 30 each comprising a local code generator, shown as PRN 36 multiplexer 32 and a low pass filter 34.

The operation of the embodiment is as follows. The received, down converted, digitised GPS signal is decimated by the decimator 26. Preferably, this is by producing a combinatorial output from groups of N samples, thereby reducing the sample rate by a factor of M. The factor M is the number of samples shifted into the decimator. Then the decimated samples are loaded into a first shift register 50 at a rate of 2.046 MHz. When the first shift register 50 is full, the input is switched to the second shift register 51 and the output of the first shift register 50 is directed by multiplexer 52 to the channels 30. The output of the first shift register is also looped back to its input. The first shift register is then circulated at a higher than normal frequency, such as 128 MHz. In each channel 30 a PRN generator 36 generates a local version of the CA code and a multiplexer 32 combines the decimated received code with the local version of the CA code. The clock of the correlators and first shift register run at the same multiple of the normal rate thereby performing many searches on the data before the second shift register 51 is full. The number of searches is given by the number of correlators x the factor higher than real time rate of the shift register. Each correlator starts its correlation at a different, evenly spaced point in the local CA code, thereby covering all possible combinations of correlation. At which point, the input is switched to the first register 50 and the multiplexer 52 switches the output of the second register 51 to the correlators.

Note the special case when the sample rate reduction, the overclocking, and the number of correlators combine to allow processing at 2046 or more times real time rate. Then all possible time-domain searches can be performed before switching buffers, so no data is lost and the correlator outputs can be further integrated by hardware or software accumulators, completely separating the integration period (and hence sensitivity) from the size of the input buffers. This greatly enhances sensitivity and reduces silicon area.

Example implementation x8 decimation, x8 clock, x16 channels, x2 correlators per channel is x 2048 real time.

The hardware can thereby perform all 2046 correlations in 1ms which is the repeat period of the CA code. This means that every 1 ms when the code repeats it can be correlated for all possible time domains.

The shift registers described could equally be implemented by other stores such as RAM with counters for addressing. Any buffer store which is capable of reading in at a first rate and reading out a sequence of digital data at a second higher rate will do.

When the signal has been acquired (the relative time difference has been calculated by the correlations) a tracking mode is entered by a select signal 53 switching the input for multiplexer 52 to provide the received, down converted digitised signal direct to the correlators.

The decimator 26 is shown in Figure 4 and comprises a shift register 60 and adder 62. In essence, the decimator sums N samples together (here 8 samples are summed) to produce an output on line 63. In this example, 8 samples of the digitised received signal are summed giving possible outputs -8 to +8. To represent the possible

outputs, the output values 0, 1, 2 or 3 are represented as logic "0" and outputs 5, 6, 7 or 8 are represented as logic "1". To prevent any bias in the output the value 4 is represented as alternately logic "0" and logic "1". The output on line 63 is therefore a digital bit sequence which is a downsampled version of the digitised received signal without any information being discarded.

The choice of 8 bit summing is apt as this is the ratio between the 16 MHz sampling of the received signal and 2 MHz of the received GPS signal. In fact, the exact figures are 16.368 MHz and 2.046 MHz being multiples of the 1.023 MHz chip rate as all the clocks in the system are synchronous.

Whilst at first sight it may appear that information is lost by summing received samples this is not the case as can be seen with reference to Figure 5. The initial sampling of the received signal is at 16 MHz (Figure 2a) producing 16 samples per CA code chip (the chip rate being 1 MHz). Thus the summing of 8 samples effectively produces 2 samples per CA code chip.

[Q. Why not initially sample at 2 MHz during acquisition - doesn't this produce the same result? A. Because that would not produce the SN benefit of summing and would lose the accuracy when tracking.]

The sampled and summed signal can therefore be correlated with the appropriately locally generated CA code to acquire the signal to within one chip (microsecond). Once acquired, the signal can be tracked to an accuracy of the 16 MHz sampling (of the order tens of nanoseconds).

Other summing ratio are possible, such as N = 4 or N = 16. In such cases, the system can remain synchronous in that

the clocks for sampling and summing are all derived by even integer division of a common clock.

The decimator could also take the form shown in Figure 6. In this form, the line >4 is logic "1" when the output of adder 70 is >4, and similarly lines =4 and <4 are asserted when the output of the adder is 4 and <4 respectively.

A dither function alternately presents 0 or 1 whenever the line =4 is asserted. The output of multiplexer 74 is thus either the >4 output or a dithered logic "0" or "1". Now as the >4 output is "0" if the sum is not >4 or "1" if the output is >4 the result is effectively the summing of 8 samples.

Further summing values for N and M are possible. An example of summing an odd number is to shift N = 8 samples at a time into a register of M = 9 bits and sum N = 8. In this example, the eight bit will be summed twice, but we now have no need to have a dither bit as a sum of 0, 1, 2, 3 or 4 is represented as logic "0" and 5, 6, 7, 8 or 9 represented as logic "1" (there are equal chances of logic "0" or "1" occurring). Similarly, division by 17 would involve values 0 to 8 being represented as logic "0" and values 9 to 17 being represented as logic "1".

Other alternatives include shifting N = 8 bits but sum N = 7 bits such that values 0 to 3 are logic "0" and values 4 to 7 are logic "1". This alternative does actually discard a sample, but has no effect on the signal to noise ratio.

[Q. Why is there no effect on SN?]
As previously described, the particular benefit is obtained when the acquisition runs at greater than 2046 real time. In this situation, the acquisition can be performed on the signal as actually received in real time.

This is 2 x 1024 (the chip length). The factor of 2 is to avoid the sampling occurring at chip boundaries which would occur in a syndronous system.

An alternative embodiment using only a single shift register is shown in Figure 7. Although not shown, there are 16 separate correlators - one for each channel. Also, the figure only shows one of the inphase (I) and quadrative (Q) channels for simplicity.

An incoming signal is mixed down by gate 44, fed with a locally generated 4.092MHz. A decimator 26 comprises combinatorial logic to combine groups of 8 samples to reduce the sample rate without discarding information as before. It is noted, for the avoidance of doubt, that the decimation is not simply removing every 10^{th} sample. The decimated signal is loaded to a shift register 28 having multiple taps 29 which feed to correlators 30. The shift register is operable, when loaded, to circulate at a higher speed than the loading speed, such as 66 MHz or 200 MHz preferably 128 MHz. Each tap 29 feeds a separate correlator 30 (only one being shown for simplicity). A code generator 36 generates a local version of the respective CA code and applies this to the correlator 30. The correlator includes combinatorial logic 32 which combines the local version of the CA code with the decimated received signal from the tap points 29 of the circulating shift register. A low pass filter 34 provides the output.

The operation of the channel 16 is in two modes; an acquire mode and a tracking mode. The acquire mode will be described first. On first receiving a satellite signal which has been sampled at 16 MHz, the timing of the satellite which sent the signal and the relative distance are both unknowns. Accordingly, it is necessary to perform 2,046 (2x1,023 chips of the CA code) comparisons

to determine the relative time difference between the local version of the CA code and the received signal. The received signal is first decimated, though, to reduce the samples by a factor of 8. The decimated samples are fed to the shift register at 2.046 MHz which then circulates at a higher speed such as 66 MHz or 200 MHz preferably 128 MHz. Each of 16 tap points 29 is fed to a respective correlator 30. The 16 correlators 30 each receive the same CA code for a given satellite from the code generator 36. There are thus effectively 16 correlators running in parallel on a signal which is reduced by a factor of 8 samples at a speed which is a multiple of the usual speed. If the speed is 66 MHz, this is 4 times faster than usual so the system is 4 x 8 = 32 times faster than 16 channels without decimation or the high speed register. If the speed is 200 MHz, this is 12 times faster than usual so that system is 12 x 8 = 96 times faster than 16 channels without decimation on the high speed register.

The increase in speed means either a faster acquisition or more sensitivity in the same time. For example, 32 times faster means 32 times more sensitive at the same acquisition speed giving around 15 dB gain.

When the signal has been acquired (the relative time difference has been calculated by the correlations) there is less need for high speed correlation. Accordingly, the channels enter a second mode; the tracking mode. In this mode the decimator 26 no longer decimates the incoming signal. The code generator 36 now supplies a different respective code to each of the 16 correlators; one for each respective satellite to be tracked. The relative positions of the incoming and local signal are now known to a degree of accuracy of a few nanoseconds rather than being unknown and so can be tracked using the early and late signals discussed before.

Whilst the second embodiment cannot operate to perform all possible correlations in real time (because the received digitised data will be at a faster rate than the correlations) the single shift register embodiment still provides some speed advantage.

CLAIMS

(01-IMS-018)

1. A semiconductor integrated circuit for processing a plurality of received broadcast signals, the broadcast signals being of the type each having a different respective ~~repeated~~ unique digital code for position calculation, comprising a digital sampler, a sample reducer and a plurality of correlators being arranged to be operable in two modes such that:

in an acquisition mode:

- the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate;
- the sample reducer reduces the bits of the digital bit stream by combining groups of N bits together to produce a reduced digital bit stream;
- the plurality of correlators receive the reduced digital bit stream at a second bit rate, being higher than the first bit rate, and each of the plurality of correlators correlates the reduced digital bit stream with the same locally generated version of one of the different repeated digital codes; and

in a tracking mode:

- the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate and provides the digital bit stream direct to each of the plurality of correlators, each correlator correlates the digital bit stream with a different locally generated version of one of the repeated digital codes.

2. A semiconductor integrated circuit according to claim 1, wherein in acquisition mode the sample reducer comprises an adder for adding the groups of N bits.

3. A semiconductor integrated circuit according to claim 2, wherein in acquisition mode the adder provides a digital output representative of the value of the sum of the N bits.

4. A semiconductor integrated circuit according to claim 3, wherein in acquisition mode the adder provides a logic "1" output if the sum of the N bits is greater than a given value and a logic "0" if the sum of N bits is less than the given value.

5. A semiconductor integrated circuit according to claim 4, wherein in acquisition mode the adder alternately provides a logic "1" and logic "0" if the output is equal to the given value.

6. A semiconductor integrated circuit according to any preceding claim, wherein in acquisition mode the second bit rate is a factor M higher than the first bit rate.

7. A semiconductor integrated circuit according to claim 6, wherein there are Y correlators such that in acquisition mode the correlation rate is a factor X = N (bits) x M (bit rate factor) x Y(correlators) faster than the correlation rate in tracking mode for one of the repeated digital codes.

8. A semiconductor integrated circuit according to claim 7, wherein the factor X is chosen to be substantial equal or greater than twice the number of bits in the repeated code, whereby all possible correlations of the code are performed before the code repeats.

9. A semiconductor integrated circuit according to claim 9, wherein the repeated digital code is a GPS position code of 1,023 bits and wherein the factor X is arranged to be 2,048.

10. A semiconductor integrated circuit according to any preceding claim, further comprising a memory for receiving the reduced digital bit stream and for outputting the reduced digital bit stream at the second bit rate to the plurality of correlators.

11. A semiconductor integrated circuit according to claim 10, wherein the memory comprises a circulating shift register.

12. A semiconductor integrated circuit according to claim 11, wherein the circulating shift register receives the reduced digital bit stream at a rate equal to the first bit rate divided by N and circulates at the second bit rate.

13. A semiconductor integrated circuit according to any of claims 10 to 12, wherein the memory comprises two shift registers arranged to alternately receive the reduced digital bit stream while another of the two shift registers circulates at the second bit rate.

14. A method of processing a plurality of received broadcast signals each having a different respective ~~repeated~~ Roam digital code for position calculation, comprising:

- sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

- reducing the bits of the digital bit stream by combining groups of N bits to produce a reduced bit stream;
- correlating the reduced digital bit stream at a second bit rate using a plurality of correlators each correlating the reduced digital bit stream with the same one of a locally generated version of the repeated digital codes to acquire the broadcast signals; and subsequently
- correlating the digital bit stream at the first bit rate using the plurality of correlators each correlating the reduced digital bit stream with a locally generated version of a different one of the repeated digital codes to track the previously acquired signals.

15. A method according to claim 14, wherein the step of reducing the bits of the digital bit stream comprises summing groups of N bits.

16. A method according to claim 15, wherein the summing produces a digital output representative of the sum.

17. A method according to claim 16, wherein the summing produces a logic "1" if the sum of N bits is greater than a given value and a logic "0" if the sum is less than the given value.

18. A method according to claim 17, wherein the summing alternately provides a logic "1" and logic "0" if the output is equal to the given value.

19. A method according to any preceding claim, wherein the second bit rate is a factor M higher than the first bit rate.

20. A method according to claim 19, wherein there are Y correlators such that when correlating to acquire the correlation rate is a factor X = N (bits) x M (bit rate factor) x Y (correlators) faster than the correlation rate when tracking the acquired signals.

21. A method according to claim 20, wherein the factor X is chosen to be substantially equal or greater than twice the number of bits in the repeated code, whereby all possible correlations of the code are performed before the code repeats.

CLAIMS

(01-IMS-019)

1. A semiconductor integrated circuit for processing a plurality of received broadcast signals, the broadcast signals being of the type each having a different respective ~~repeated~~ known digital code for position calculation, comprising: a digital sampler, a memory arrangement and a plurality of correlators, being arranged to be operable in two modes such that:

in an acquisition mode:

- the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate;
- the memory arrangement receives the digital bit stream and outputs at a second bit rate, being higher than the first bit rate;
- the plurality of correlators receive the digital bit stream at the second bit rate, and each of the plurality of correlators correlates the reduced digital bit stream with the same locally generated version of one of the different repeated codes; and

in a tracking mode:

- the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate and provides the digital bit stream direct to each of the plurality of correlators, each correlator correlates the digital bit stream with a different locally generated version of one of the repeated digital codes.

2. A semiconductor integrated circuit according to claim 1, wherein the memory comprises a circulating shift register.

3. A semiconductor integrated circuit according to claim 2, wherein the circulating shift register receives the digital bit stream at a rate equal to the first bit rate and circulates at the second bit rate.

4. A semiconductor integrated circuit according to any preceding claims, wherein the memory comprises two shift registers arranged to alternately receive the digital bit stream while another of the shift registers circulates at the second bit rate.

5. A method of processing a plurality of received broadcast signals each showing a different respective digital code for position calculation, comprising:

- sampling the received broadcast signals to produce a digital bit stream at a first bit rate;
- providing the digital bit stream at a second bit rate by reading into a memory arrangement at one bit rate and reading out at the second bit rate;
- correlating the digital bit steam at the second bit rate using a plurality of correlators each correlating the reduced digital bit stream with a same one of a locally generated version of the repeated digital codes to acquire the broadcast signals; and subsequently
- correlating the digital bit stream at the first bit rate using the plurality of correlators each correlating the reduced digital bit stream with a locally generated version of a different one of the repeated digital codes to track the previously acquired signals.

6. A method according to claim 5, wherein the step of providing the digital bit stream at the second bit rate comprises circulating successive portions of the bit stream in a circulating shift register at the second bit rate.

7. A method according to claim 5 or 6, wherein the step of providing the digital bit stream at the second bit rate comprises alternately reading the bit stream into one of two shift registers while the other of the two shift registers circulates at the second bit rate.

OLD CLAIMS
(01-IMS-018)

1. A semiconductor circuit arrangement for processing a received signal, the signal being of the type having a repeated code for position calculation, comprising:

- a code generator arranged to generate a local version of the repeated code;
- a plurality of correlators arranged to receive the local version of the repeated code;
- a decimator configured to sample the received signal to combine groups of N bits to thereby reduce the bits in the code by the factor N; and
- whereby the correlators perform correlations at a factor N of the usual rate.

OLD CLAIMS
(01-IMS-019)

1. A semiconductor circuit arrangement for processing a received signal, the signal being of the type having a repeated code for position calculation, comprising:

- a code generator arranged to generate a local version of the repeated code;
- at least one correlator arranged to receive the local version of the repeated code; and
- two buffer stores arranged to alternately read in and store the received signal at a first rate and read out the received and stored signal at a second rate, the second rate being a multiple of the first rate.

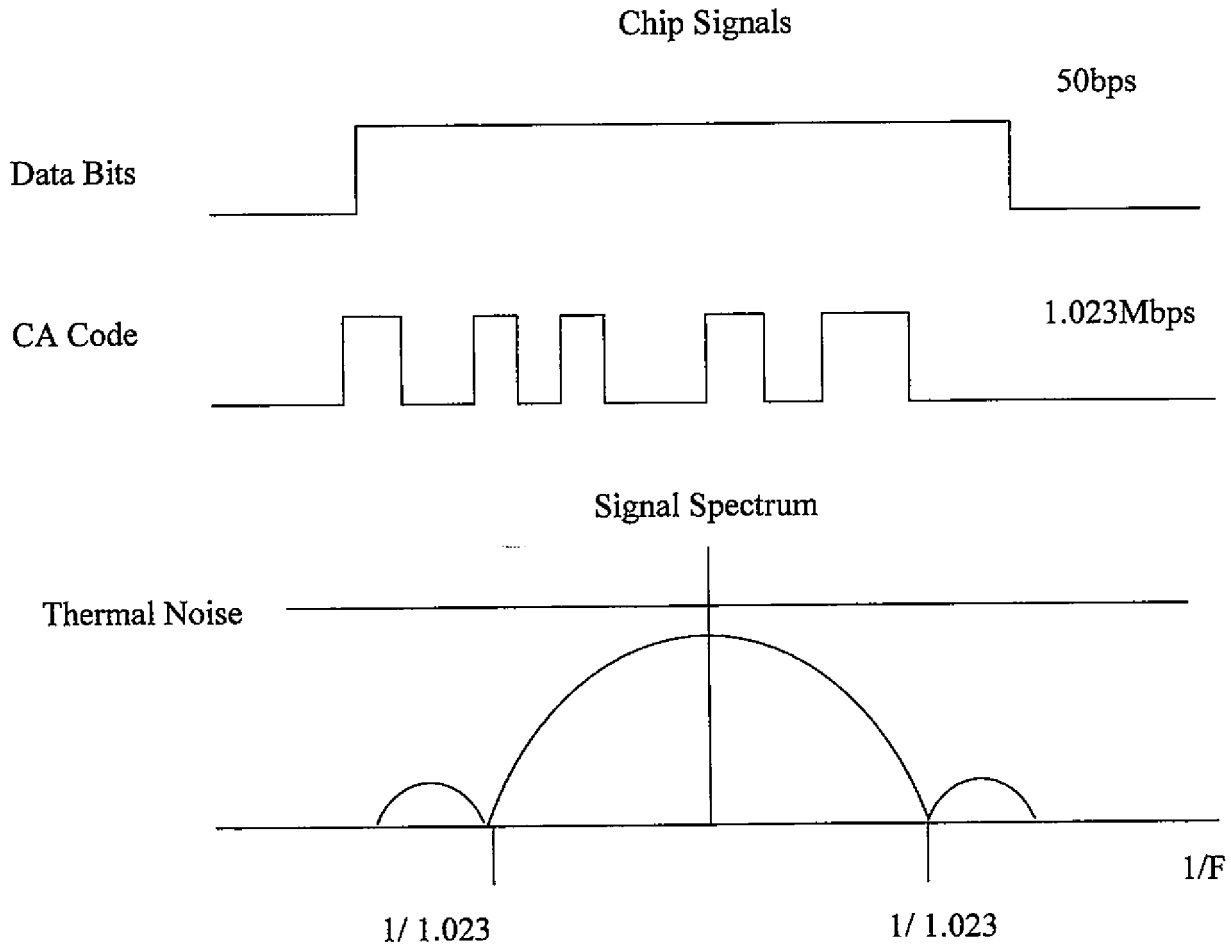
Chip Signals
50bps
Data Bits
CA Code
1.023Mbps
Signal Spectrum
Thermal Noise
1/F
1/ 1.023
1/ 1.023

Figure 1

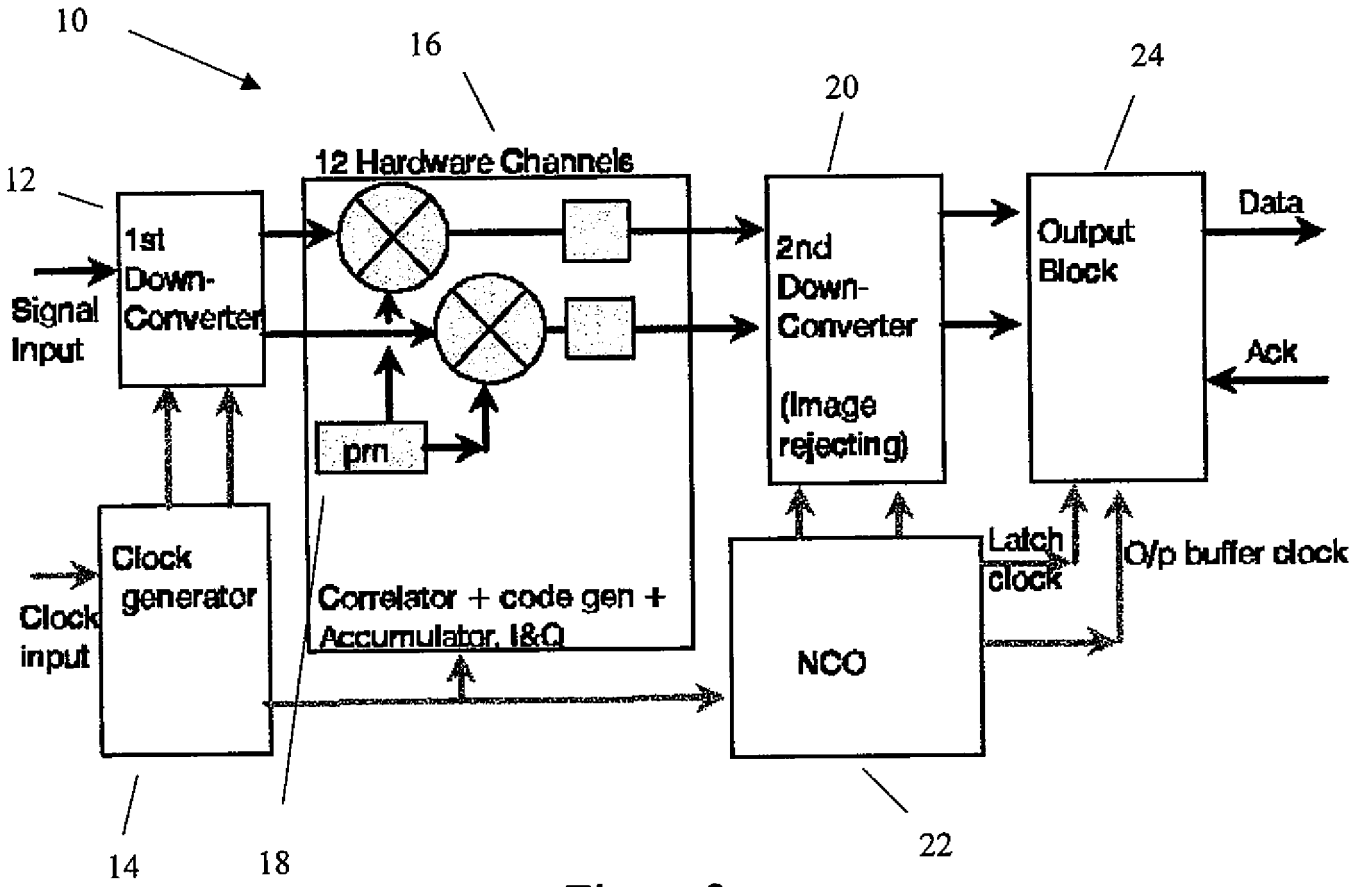
10
16
20
24
12
12 Hardware Channels
1st
Down-
Converter
Signal
Input
2nd
Down-
Converter
(Image
rejecting)
Output
Block
Data
Ack
prn
Clock
generator
Clock
input
Correlator + code gen +
Accumulator, I&Q
NCO
Latch
clock
O/p buffer clock
14
18
22

Figure 2

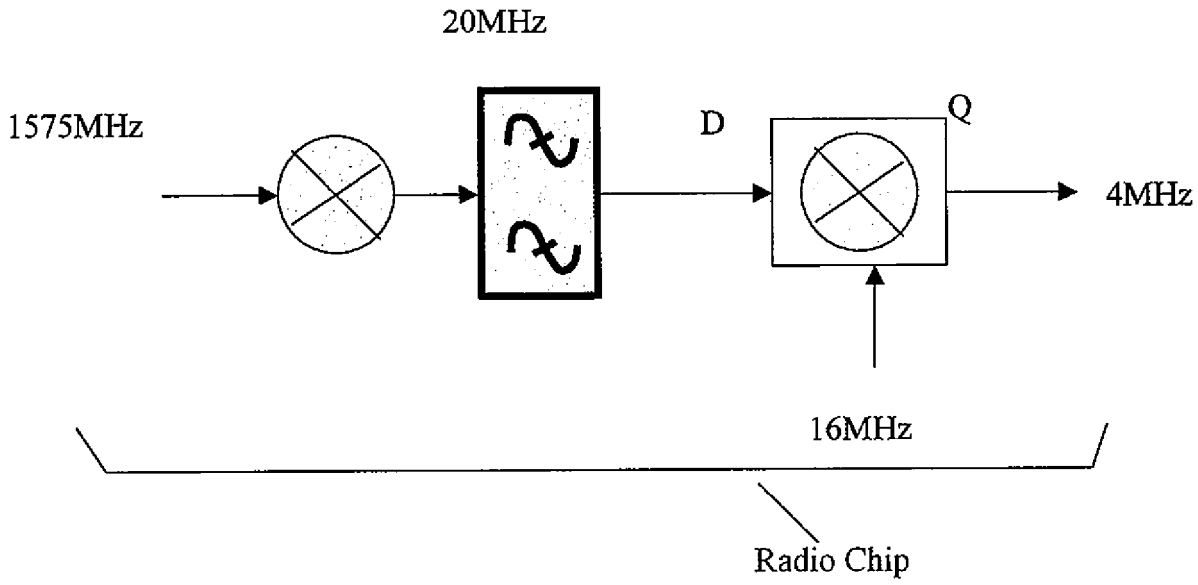

Figure 2a

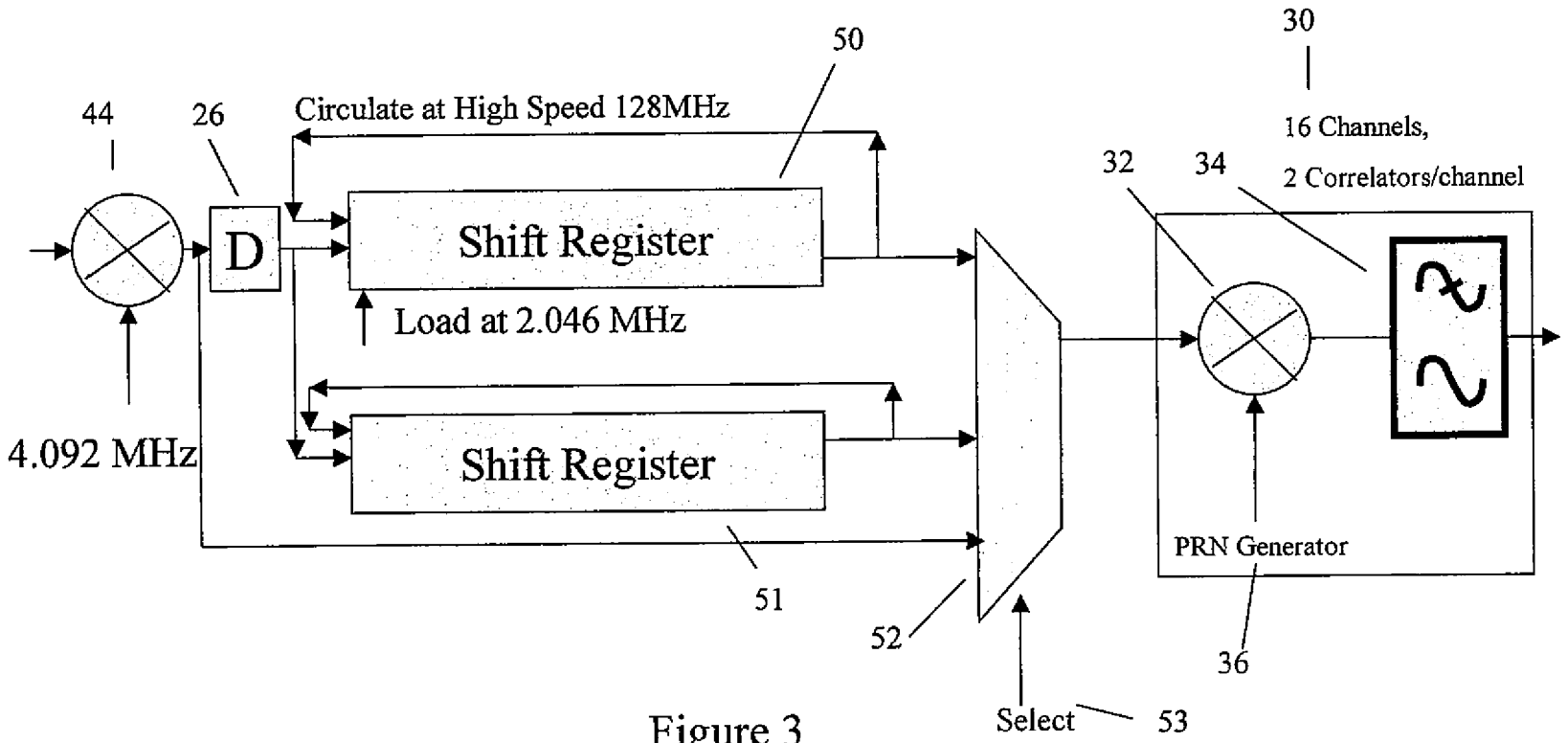
30
50
44
26
Circulate at High Speed 128MHz
16 Channels,
2 Correlators/channel
32
34
D
Shift Register
Load at 2.046 MHz
4.092 MHz
Shift Register
PRN Generator
51
52
36
Select
53

Figure 3

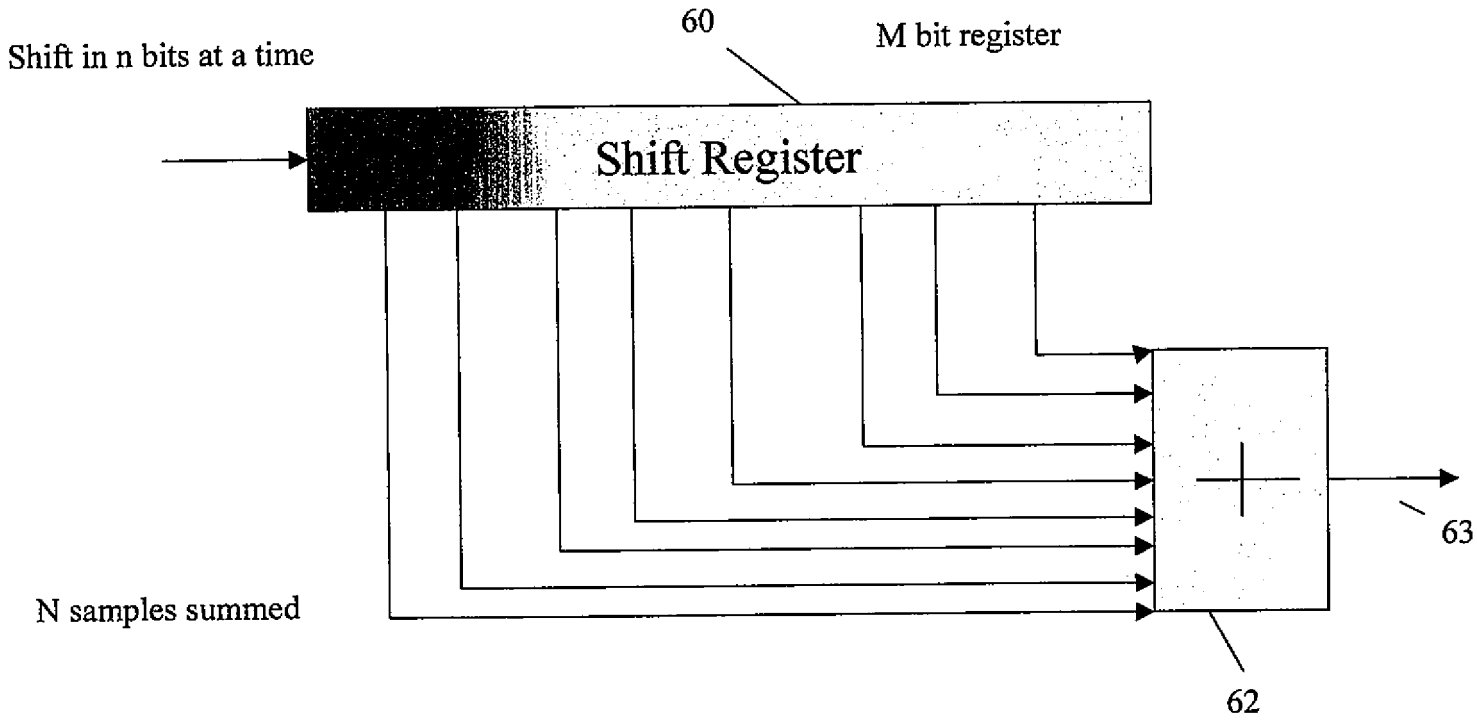
Shift in n bits at a time
60
M bit register
Shift Register
63
N samples summed
62

Figure 4

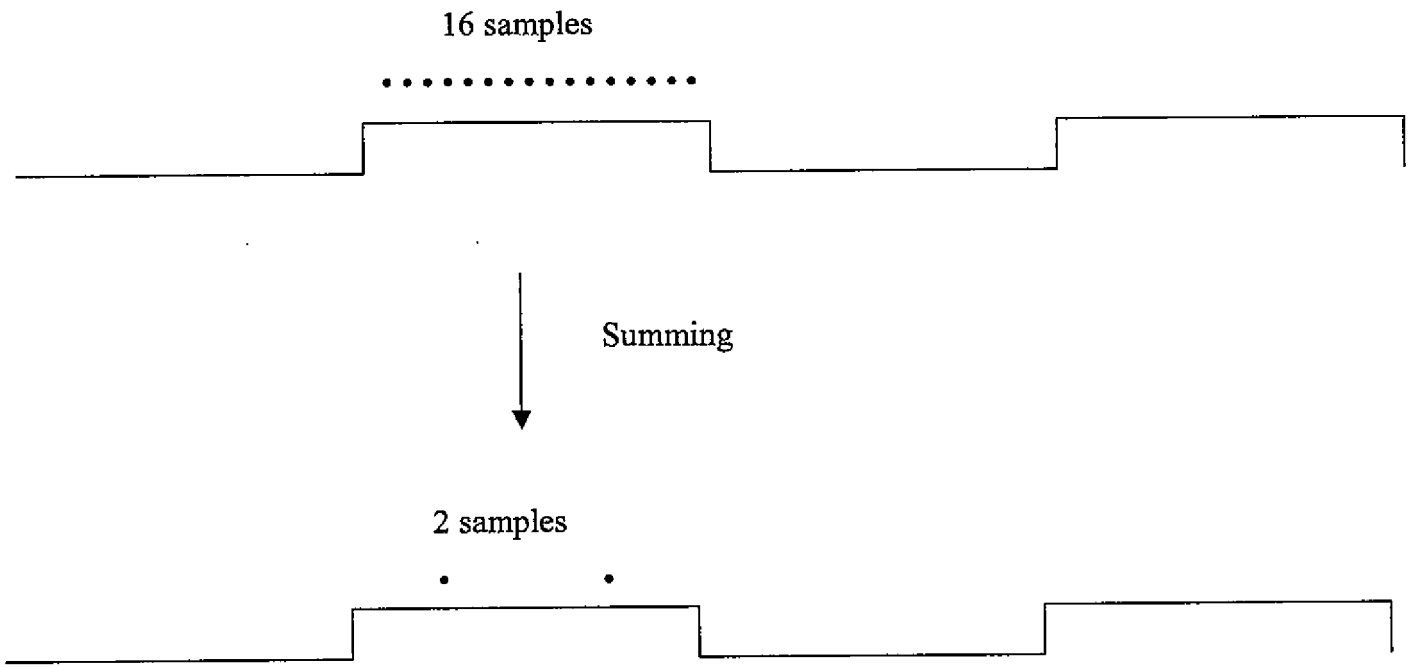

Figure 5

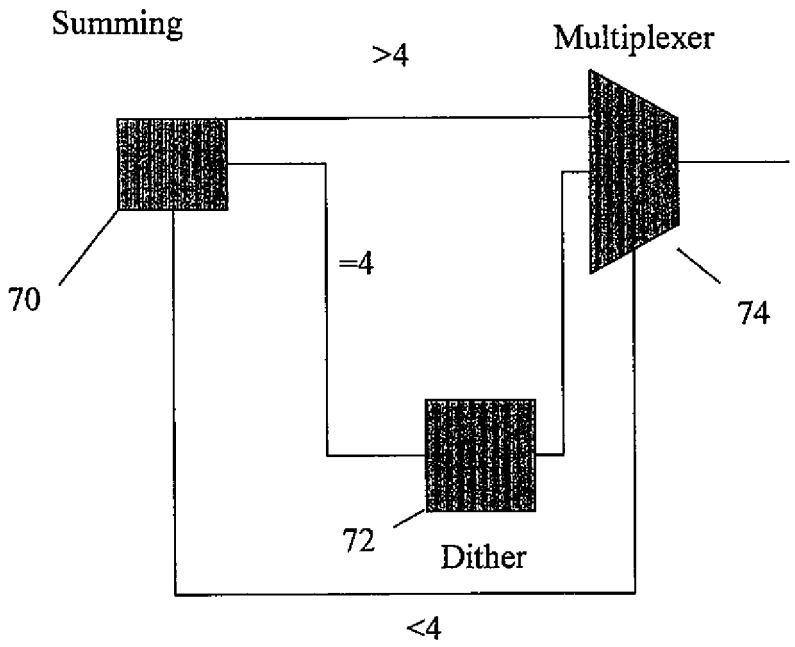

Figure 6

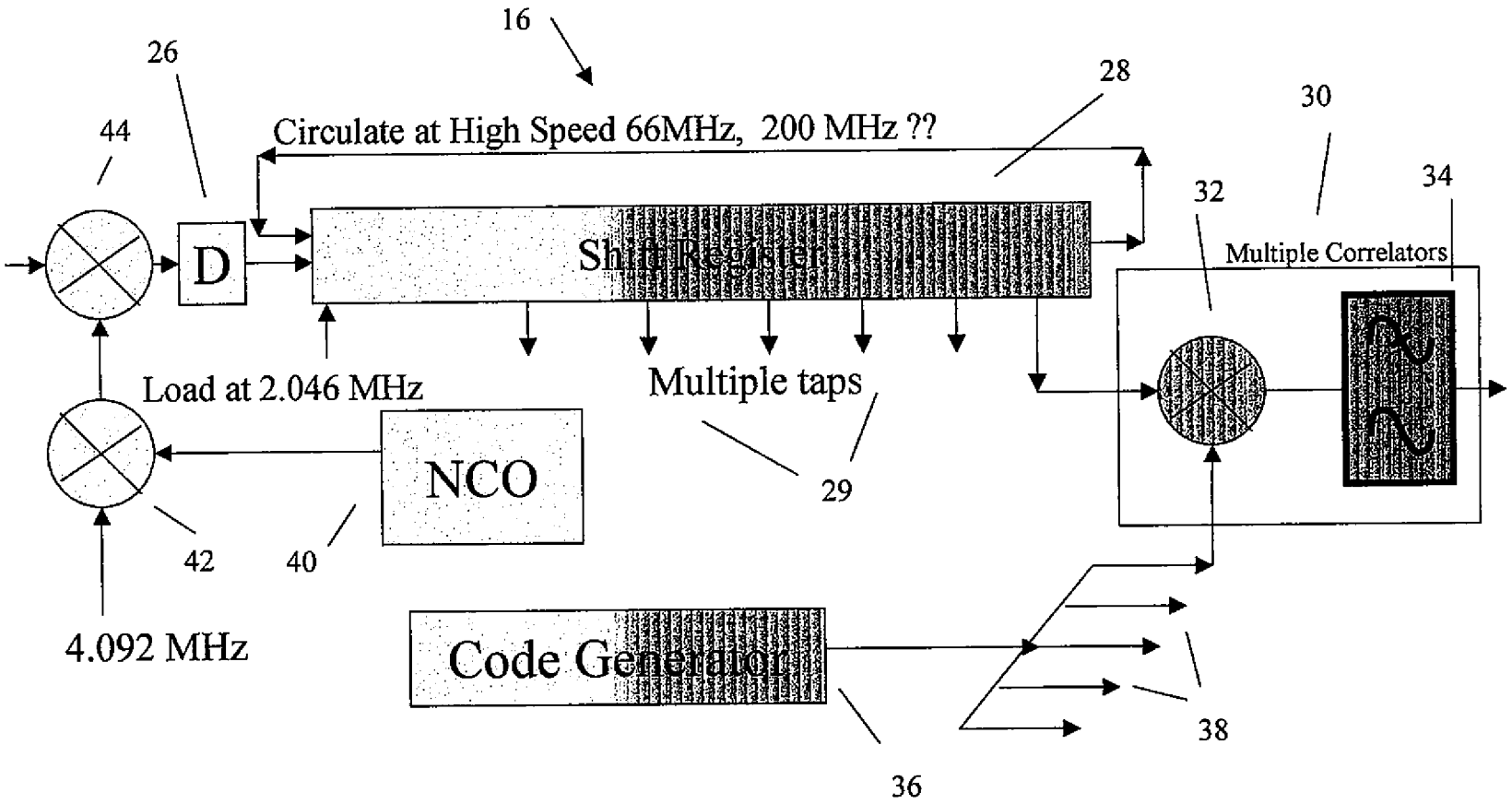
16
26
28
30
44
Circulate at High Speed 66MHz, 200 MHz ??
32
34
D
Shift Register
Multiple Correlators
Load at 2.046 MHz
Multiple taps
NCO
29
42
40
4.092 MHz
Code Generator
38
36

Figure 7